UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,711	11/12/2003	Shridhar Mukund	ADAPP222	9276

25920	7590	04/17/2006

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EXAMINER
LO, SUZANNE

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/712,711	MUKUND ET AL.
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>12 November 2003</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-19</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-19</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>12 November 2003</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>5/20/04 4/4/05 5/9/05</u>

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 7-05)　　　　　　　　Office Action Summary　　　　　　　　Part of Paper No./Mail Date 04042006

DETAILED ACTION

1.   Claims 1-19 have been presented for examination.

PRIORITY

2.   Acknowledgment is made of applicant's claim for priority to provisional application 60/433,490

filed on 12/12/2002.

Information Disclosure Statement

3.   The information disclosure statements (IDS) submitted on 05/20/2004, 04/04/2005 and

05/09/2005 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has

considered the IDS' as to the merits.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition
> of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
> conditions and requirements of this title.

4.   Claims 1-4 and 9-19 rejected under 35 U.S.C. 101 because the claimed invention is directed to

non-statutory subject matter.

Specifically, claims 1-4, 9, 11-12, 14-18 do not produce a tangible result. The claims do not

enable their usefulness to be realized, there is only definition, generation, comparison, and identification

being performed and there is no display or an output generated from the identification.

Specifically, claims 9-14 are directed to software, *per se*, which is abstract. Claims 9-14 are

written so broadly they do not have to include hardware, only software.

Specifically, claims 15-19 are directed to non-statutory computer readable medium. The

machine-accessible medium includes non-statutory medium, specifically electrical or magnetic signals as

stated on lines 8-14, page 19 of the specification. The medium must be limited to tangible, statutory

computer-readable medium.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5.   Claim 5 recite the limitation "the method operation" in the first line of the claim. There is

insufficient antecedent basis for this limitation in the claim given the situation that in claim 1, the

comparison of the signals is acceptable.

6.   Claim 10 recites the limitation "the logic for identifying a cause" in the first line of the claim.

There is insufficient antecedent basis for this limitation in the claim given the situation that in claim 9, the

comparison of the signals is acceptable.

7.   Claim 19 recites the limitation "the program instructions for identifying a cause" in the first and

second lines of the claim. There is insufficient antecedent basis for this limitation in the claim given the

situation that in claim 15, the comparison of the signals is acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis

for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8.   **Claim 1-6, 9-12, and 14-19 are rejected** under 35 U.S.C. 102(e) as being clearly anticipated by

Shimogori et al. (U.S. Patent Application No. 2002/0152061A1).

As per claim 1, Shimogori is directed to a method for simulating a chip circuit ([0053]), comprising: defining a library of components for a processor ([0083]); defining interconnections for a set of pipelined processors including the processor ([0047]); generating a processor circuit by combining the library of components and the interconnections for the set of pipelined processors ([0083]); generating a code representation of a model of the set of pipelined processors ([0058]); and comparing signals generated by the code representation to signals generated by the processor circuit ([0062]), wherein if the comparison of the signals is unacceptable, the method includes, identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit ([0090]).

As per claim 2, Shimogori is directed to the method of claim 1, wherein the library of components is included as register transfer logic (RTL) ([0053]).

As per claim 3, Shimogori is directed to the method of claim 1, wherein the interconnections for the set of pipelined processors is included in a structural netlist ([0099]).

As per claim 4, Shimogori is directed to the method of claim 1, wherein the set of pipelined processors are configured to manipulate layers of a header of a data packet in stages ([0068]).

As per claim 5, Shimogori is directed to the method of claim 1, wherein the method operation of identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes, inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals ([0091]).

As per claim 6, Shimogori is directed to a method for debugging a processor circuit, comprising: identifying a block level location having an error from a first simulation ([0090]); inserting a patch into a thread specific to the block level location of the error ([0091]); executing the simulation to determine a signal level location of the error through information generated by the patch ([0091]); and correcting a code representation of a processor associated with the error ([0093]).

As per claim 9, Shimogori is directed to an apparatus for simulating a chip circuit ([0053]),

comprising: logic for generating a processor circuit by combining a library of components and defined

interconnections for a set of pipelined processors ([0083], [0047]); logic for generating a code

representation of a model of the processor ([0058]); and logic for comparing signals generated by the

code representation to signals generated by the processor circuit ([0062]), wherein if the comparison of

the signals is unacceptable, the logic for comparing signals includes, logic for identifying a cause of the

unacceptable comparison of the signals at a block level of the code representation ([0090]).

As per claim 10, Shimogori is directed to the apparatus of claim 9, wherein logic for identifying

a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes,

logic for inserting a patch into the code representation to identify a signal level location for the

unacceptable comparison of the signals ([0091]).

As per claim 11, Shimogori is directed to the apparatus of claim 9, wherein the library of

components is included as register transfer logic (RTL) ([0053]).

As per claim 12, Shimogori is directed to the apparatus of claim 9, wherein the interconnections

for the set of pipelined processors is included in a structural netlist ([0099]).

As per claim 14, Shimogori is directed to the apparatus of claim 9, wherein each logic

component is one of hardware and software ([0101]).

As per claim 15, Shimogori is directed to a computer readable medium ([0101]) having program

instructions for simulating a chip circuit, comprising: program instructions for defining a library of

components for a processor ([0083]); program instructions for defining interconnections for a set of

pipelined processors including the processor ([0047]); program instructions for generating a processor

circuit by combining the library of components and the interconnections for the set of pipelined

processors ([0083]); program instructions for generating a code representation of a model of the set of

pipelined processors ([0058]); and program instructions for comparing signals generated by the code

representation to signals generated by the processor circuit ([0062]), wherein if the comparison of the signals is unacceptable, the computer readable medium includes, program instructions for identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit ([0090]).

As per claim 16, Shimogori is directed to the computer readable medium of claim 15, wherein the library of components is included as register transfer logic (RTL) ([0053]).

As per claim 17, Shimogori is directed to the computer readable medium of claim 15, wherein the interconnections for the set of pipelined processors are included in a structural netlist ([0099]).

As per claim 18, Shimogori is directed to the computer readable medium of claim 15, wherein the set of pipelined processors are configured to manipulate layers of a header of a data packet in stages ([0068]).

As per claim 19, Shimogori is directed to the computer readable medium of claim 15, wherein the program instructions for identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes, program instructions for inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals ([0091]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966),

that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are

summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9.   **Claims 7, 8, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimogori et**

al. (U.S. Patent Application No. 2002/0152061A1) **in view of Shridhar et al. (U.S. Patent No.**

5,815,714).

As per claim 7, Shimogori is directed to the method of claim 6, but fails to disclose wherein the

patch is a print command. Shridhar teaches inserting a print command to determine the signal level

location of an error **(column 4, lines 40-42)**. Shimogori and Shridhar are analogous art because they are

from the same field of endeavor, testing and debugging code. It would have been obvious to one of

ordinary skill in the art at the time of the invention to combine the chip circuit simulation method of

Shimogori with the debugging print commands of Shridhar in order to provide convenient means for

modifying the underlying source code as required **(column 3, lines 44-47)**.

As per claim 8, Shimogori is directed to the method of claim 6, but fails to disclose wherein the

method operation of executing the simulation to determine a signal level location through information

generated by the patch includes, triggering a print statement indicating the signal level location of the

error. Shridhar teaches inserting a print command to determine the signal level location of an error

(column 4, lines 40-42). Shimogori and Shridhar are analogous art because they are from the same field

of endeavor, testing and debugging code. It would have been obvious to one of ordinary skill in the art at

the time of the invention to combine the chip circuit simulation method of Shimogori with the debugging

print commands of Shridhar in order to provide convenient means for modifying the underlying source

code as required **(column 3, lines 44-47).**

As per claim 13, Shimogori is directed to the apparatus of claim 10, but fails to disclose wherein

the patch includes logic for executing a print statement. Shridhar teaches inserting a print command to

determine the signal level location of an error **(column 4, lines 40-42).** Shimogori and Shridhar are

analogous art because they are from the same field of endeavor, testing and debugging code. It would

have been obvious to one of ordinary skill in the art at the time of the invention to combine the chip

circuit simulation method of Shimogori with the debugging print commands of Shridhar in order to

provide convenient means for modifying the underlying source code as required **(column 3, lines 44-47).**

Conclusion

10.   All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should

be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be
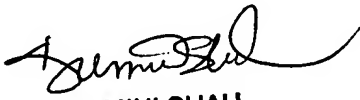
reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this

application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be obtained

from either Private PAIR or Public PAIR. Status information for unpublished applications is available

through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Suzanne Lo
Patent Examiner
Art Unit 2128

SL
04/06/06

KAMINI SHAH
SUPERVISORY PATENT EXAMINER